Available Techniques for Magnetic Hard Disk Drive Read Channel Equalization

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ABSTRACT

This paper presents an extensive, non-exhaustive, study of available hard disk drive read-channel equalization techniques used in the storage and readback of magnetically stored information. The physical elements and basic principles of the storage processes are introduced together with the basic theoretical definitions and models. Both read and write processes in magnetic storage are explained along with the definition of simple key concepts such as user bit density, intersymbol interference, linear and areal density, read head pulse response models, and coding algorithms.

The building blocks of disk drive electronics are succinctly described. The main read channel architectures: partial-response maximum likelihood (PRML) and Decision Feedback Equalization (DFE) based systems, are described and compared. Two continuous-time practical solutions are presented for the forward equalizer (the critical block of the system) in the MDFEs architecture. Recursive adaptive continuous-time filters based on gm-C topology are proposed for the implementation of the equalizer. An orthonormal state-space recursive current mode filter is proposed and compared at transistor level to a companion-form canonical structure. The basic circuits for the implementation of building blocks are presented and compared to existing solutions. A self-biased transconductance cell is presented for the implementation of very high frequency current mode gm-C filters using biased MOSFET capacitor arrays in standard digital CMOS technology.

1. BASIC PRICIPLES OF MAGNETIC HARD DISK DRIVE SYSTEMS

Magnetic support has long been the prime choice for non-volatile data storage. The physical characteristics of magnetic disk devices are a fine match for the requirements of fast and non-sequential recording and playback of digitally stored data, pushing its performance way beyond its magnetic storage counterparts in all relevant parameters. Mass production of desktop and laptop computers has quickly led magnetic disks from 3.5" multi-disk bays to single-platter 2.5", 1.8" or even 0.85" disk drives with the traditional architecture scaled to fit a thumbnail, defying even the obvious appeal of massive non-volatile solid state disks (SSD) or flash memories.

Hard disk drives (HDD) store data by magnetizing a thin 10–30nm ferromagnetic film coating on an endurable physical foothold, usually a platter made of aluminium alloy or glass/ceramics. The magnetic tracks on the media surface are narrow concentric rows of very small magnets containing user information. Earlier designs using magnetic film surface veneers can easily fit several thousand circular concentric tracks[1] per centimetre (or up to a million in later and more advanced designs). A conventional track can pack more than 200 kbit per inch in slight individual magnetic records (linear bit density) or up to 1 Mbit per inch for perpendicular to platter recording. Each of these magnetic dipoles are used to hold and playback non-volatile data.

The user bit[2] is recorded on the disk surface driven by a magnetic flux throughput imposed on the magnetic head during the write process. Once stored on these tiny independently oriented magnets, the bit can be sensed during playback as a very low amplitude[3] voltage pulse that is subsequently processed and transmitted by the read circuitry back to the data bus via the host interface controller.

Regardless of its size, the basic physical components of a magnetic disk storage apparatus are depicted in figure 1. A magnetic disk device mainly consists of four basic physical components: spindle motor, platter (the aluminium disk), servo actuator, and read head.

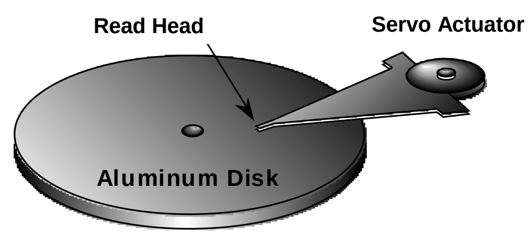


Figure 1. Physical components of a magnetic hard disk drive storage system

HDDs usually have two electric motors: one for the spindle, and the other serving as a servo actuator for the read head arm. The spindle motor is used to steer the movement of the disk(s), spinning its angular velocity up to more than 10000 revolutions per minute (rpm) for high performance disks, and is accountable for about 40% of the total disk drive power. The head actuator or servo actuator arm, is responsible for the accurate positioning of the magnetic head over a random track on the disk. The inductive head hovers over the surface of the disk, at the end of the actuator arm. It is usually made of a microscopic magneto-sensitive alloy embraced by a coiled wire.

[1] The tracks are further divided in angle defined portions called sectors, each having data and header servo fields for correct track positioning and monitoring, gain setting and clock recovery.

[2] Logical 1 if there is a transition on flux magnetization (either left to right or right to left) and logical 0 if no transition occurs.

[3] The raw output pulses induced on the read head have approximately 1mVpp.

Older disk systems used conventional inductive C-shaped or metal in gap (MIG) read heads in which the flux flows parallel to the film coating on the disk surface. The use of magnetoresistance (MR) and giant magnetoresistance (GMR), and of thin film read heads optimized and further separated the read and write process, but only with the introduction of tunnelling magnetoresistance (TMR) and perpendicular magnetic recording (PMR) in 2005, the orientation of the flux from the read head changed from parallel to perpendicular to the film coating thus allowing even tighter magnetic packing up to 1Tbit per square inch (areal density). Even though this has major implications to the write process, especially to the head structure and magnetic disk media, it has no significant impact on the read process, neither on the read sensor nor on the read channel.

1.1 Disk-drive electronic blocks

The read/write process is long and complex, starting out on the CPU all the way to the media magnets and vice versa, several electronic blocks are necessary to assure proper bit detection. Figure 2 depicts the functional diagram of all the electronic blocks involved in most disk drive system architectures.

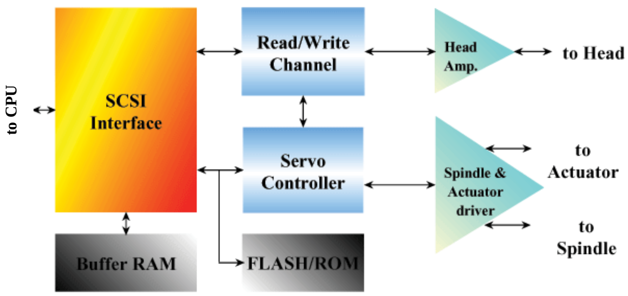


Figure 2. Physical components of a magnetic disk drive storage system

The basic building blocks are the host interface DSP[4], the read/write channel and the servo controller[5]. These blocks are usually assisted by a head amplifier[6], and by a spindle and actuator motor driver[7] front-end IC, along with some auxiliary elements for non-volatile and short-term memory. Consistent endeavour for cheaper solutions in the last decade have reduced the number of required integrated circuits from a dozen components including ASICs to just three or four ICs, corresponding to the functional blocks.

The read/write channel is the fundamental mixed signal analog/digital block of HDD electronics and is composed of two separate channels: the read channel extracts the clock, equalizes de input read head pulse, makes the digital decision and decodes data; the write channel basically encodes data. This work is focused on the read channel, and particularly, on its key component, the pulse-slimming equalizer. The equalizing target of the system is strongly dependent on the magnetic head response, and hence, on the physical properties of the playback and write processes.

1.2 Playback process

The playback process is usually originally initiated by the CPU and issued onto the disk electronic blocks through a SCSI or IDE bus controller IC. The host interface controller forwards the order to the servo controller, which in turn positions the head actuator onto the designated track, according to the track ID stored on the servo sectors. Once the head is in a fixed position, the rotating movement of the disk allows that the read channel IC can correctly access and feedback the stored user data to the host interface controller[8].

The relative movement of the stored magnets on the disk's surface in respect to the read head causes a variation of the magnetic flux that flows through the head core. The changes in the direction of magnetization represent encoded binary data bits, hence the variation in time of the magnetic flux density flow through an electric circuit wire loop coiled on the read head generates an electric field, as results from Faraday's law expressed in its integral form by

$$v(t) = -\frac{d\phi}{dt}. \qquad (1)$$

The properties of the communication channel, including read head characteristics and the physical ground rules of the read/write process can be treated as reasonably linear and time invariant. Therefore, a proper linear time-invariant system can be used to model the physical medium of the channel. The step response of the read back procedure is easy to extract based upon measured data from a specific physical medium to a stored positive transition, i.e. a specific head and media can be fully characterized from the analysis of a single flux transition.

1.2.1 Read head model

The Lorentzian model is the most widely used step response model of the playback process in recording systems. The commonly used equation for the Lorentzian pulse model shown in (2) is a good approximation for most of the referred magnetic read heads response to a positive transition in magnetic flux polarity.

$$s(t) = \frac{1}{1+\left(\frac{2\cdot t}{pw50}\right)^2} \qquad (2)$$

The model is normalized to unitary peak value, and constant *pw50* denotes the pulse width at 50% of its peak value. The corresponding pulse is depicted in figure 3, along with other common pulse shapes often used in signal processing, such as sinc, Gaussian or modified

[4] The host interface is a digital IC that controls the data interface between the read/write channel and the CPU, handling interrupts, and data transfer protocols common to magnetic or solid-state drives. Auxiliary buffer RAM is used for caching and queuing data, providing long data-bursts to improve speed and reduce bus latency.

[5] The servo DSP calculates actuator trajectories and controls the spindle and actuator driver to correctly position and maintain the read head on track.

[6] The head pre-amplifier is a 40dB gain wideband single chip device usually mounted close to the read head, driving the head during the write process and amplifying the input pulse during the read process, yielding approximately 25dB of SNR.

[7] The spindle and actuator driver is a power IC responsible for driving the head actuator and the spindle motor, it is usually implemented with power CMOS, and its consumption is about 10% of the total power needs.

[8] The elapsed time between data request and data ready at the bus is defined as the access time of the disk, usually in the order of 10 to 20 milliseconds. In most cases, the host interface controller buffers the read data in local memory, before sending it back to the host processor. This is also usually combined with sophisticated software disk caching schemes.

Lorentzian. In this model, $t=0$ corresponds to the instant that the read head hoverflies the boundary region of two adjacent magnets of opposite polarities, and hence, for maximum efficiency, most read channel architectures use clock recovery schemes to precisely sample and decide at this instant.

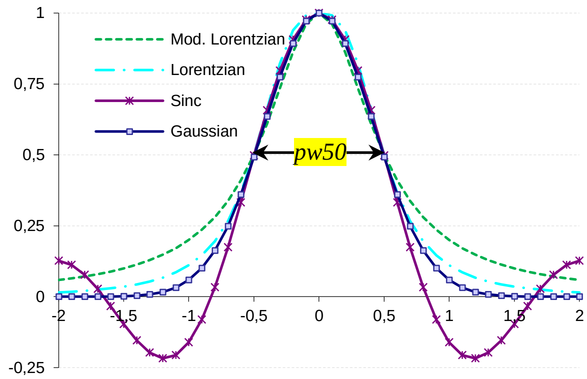


Figure 3. Read head pulse model (Lorentzian)

The portion of the response obtained for negative instants (precursor) reflects the physical fact that the influence of flux transition is sensed by the read head before it actually reaches the transition boundary, thus, since this effect precedes the optimum sampling instant, it effectively corresponds to a prior awareness of a future event, and therefore is inherently non-causal. This portion of the response is usually referred to as precursor response. Likewise, the postcursor response designates the part of the pulse that follows the transition instant. The superimposition of two consecutive flux transitions denoting consecutive ones, usually designated as dipulse or dibit response, represents the effect of allowing Inter Symbolic Interference (ISI) to occur between adjacent bits, and is frequently used to characterize the response of the read channel.

These physical constrains together with the thrust for slimmer pulses determine the dimensions of the head and justify their fabrication process, but the growing need for higher data storage densities and increased data rates have forced the use of complex circuitry systems to compensate for the amount of allowed ISI. User bit density (UBD) is defined as the pw50/T ratio, where T denotes time (or distance) between consecutive bits. High-speed acquisition and sharpening of the magnetic-head data input-pulses, is done mainly at the expense of high silicon area (thus high cost) and (unfortunately) high power consumption especially on high frequency channels. However, very slim digital bits allowing huge areal density are the essence of mass data storage, hence, different techniques are employed in data coding for the achievement of optimal performance either in data rate, error probability, noise immunity and ISI forbearance. Several coding procedures and data constrains have been used (and even combined) in magnetic read channels as a result of this effort, and the read channel topology greatly depends on the chosen coding strategy as will be shown.

1.2.2 Coding techniques

One of the most common coding schemes widely employed in data coding, especially in optical and magnetic recording is Run-Length Limitation (RLL). This coding technique[9] is characterized by two integer constrains (d,k). The d constrain avoids consecutive transitions between different symbols, thus assuring at least $d+1$ consecutive zeros or ones when a transition occurs. This constrain reduces the maximum bit rate and storage capacity, but allows the increase of the operating frequency whilst dropping speed requirements for crucial circuit blocks. The use of RLL (1,7) became typical in disk drive systems although it reduces user data rate to 2/3, since it maps 2 bits on to 3 bits. The k constrain avoids long unvarying sequences of consecutive zeros or consecutive ones, that can lead to the loss of synchronism between the clock recovery circuitry driving the detection block and the transmitted data. This is a typical problem of asynchronous data transmission systems[10] and usually has little influence on data rate.

1.3 Write process

The write process is also triggered when the host interface controller receives an order from the host processor, commanding that a given data sequence is stored onto the disk. Typically, some or all of the data will be transferred in advance, packed into blocks and buffered locally. As described for the read process, the servo controller as to position the head actuator onto a designated track. Once the head is in position, the write bits are forwarded to the write channel where they are encoded and output via the magnetic head driver to the head, through which they are forced onto the rotating disk[11].

The basic principal behind non-volatile recording of a bit on the surface of a magnetic disk is the establishment of a magnetic field imposed by an electric current flow through an electric wire. The fundamental law relating magnetic field strength and electric currents is the well-known Biot-Savart law. The current flow on the wire coiled around the magnetic head generates a magnetic field. Assuming a saturation recording system, the magnetic flux is proportional to the write current as given by

$$\phi = L \cdot I \,. \tag{3}$$

As the magnetic field is forced onto and through the disk surface, it is enduringly stored as magnetically oriented magnets with negative or positive polarity depending on the value of the stored

[9] The ***d* constrain** • *minimum run-length constrain*, imposes that transitions between different symbols occur at least $d+1$ apart from each other.

The ***k* constrain** • *maximum run-length constrain*, imposes that a transition between different symbols occurs at most k symbols after the previous one.

[10] NRZI coding codes zeros as *no-transition* and ones as *sign-transitions*, only a long series of zeros would inevitably lead to the loss of synchronism. A limitation must be imposed on the allowed length between ones, therefore at most k consecutive zeros can occur. In any case consecutive sequences of ones are not tolerable in NRZI coding due the d constrain.

[11] The physical constrains determining the access time during the write procedure are similar to the referred for the playback process. Access time can be up to 100 times smaller in solid state disks when compared with magnetic HDD, but these can cost 10 times more.

bit. The value of the magnetic flux density $\vec{B}$ vector can be precisely imposed on the ferromagnetic layer, and can be derived from

$$\phi = \iint_S \vec{B} \cdot \vec{N} \, dS \, . \tag{4}$$

For enhanced behavior some systems include a non-linear distortion at the beginning of the current pulse during the write process. This is meant to increase the initial slope of the stored pulse, thus accounting for a significant reduction of non-causal intersymbol interference. This technique is designated as write pre-compensation. This can considerably alter the pulse shape displacing signal power from the beginning of the pulse to the pulse center, and pulse tail, thus it can slightly increase causal intersymbol interference that can be in term compensated using appropriate filtering.

2. STATE OF THE ART OF READ CHANNEL ARCHITECTURES

The first solutions in magnetic hard disk drive storage for personal computers were proposed in 1980 closely followed by the first 3½" floppy drives in 1981. Early designs used conventional peak-detection read channels, basically relying on the zero crossing of the differentiated input signal, to sample the input at its local minimum or maximum value. These designs have gradually evolved to present days, and now usually include equalizer blocks with high frequency boost for pulse-slimming and more complex clock recovery schemes. Nevertheless, more advanced read channel architectures based on partial-response and more recently DFE based systems have taken the place of peak detection techniques.

2.1 Peak detection read channels

Peak detection has been the conventional technique for data acquisition, and the main market solution for several decades for the read channel since the appearance of disk drives. This scheme combines the lowest implementation cost with high efficiency in RLL encoded channels, especially for low-density disks. The peak-detector block depicted in figure 4 is the key functional block of this read channel.

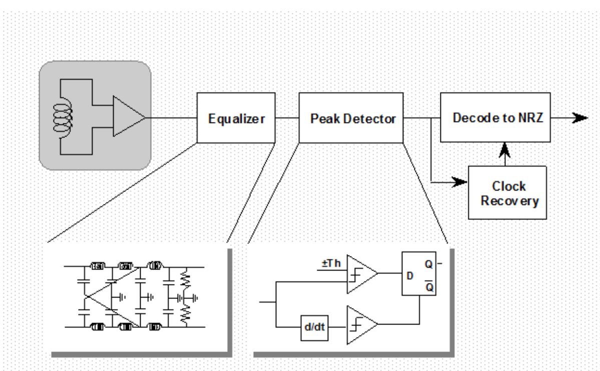


Figure 4. Peak detection read channel block diagram

This block differentiates the input signal from the read head amplifier, and uses a simple comparator set to ground, thus identifying zero crossing. The output of the comparator clocks a flip-flop circuit ideally sampling the input signal at its local minimum or maximum value, the sampling instant is centered on the timing window with acceptably high accuracy and noise immunity. A peak is detected if the module of the input value is greater than a threshold voltage (usually half the maximum amplitude), thus corresponding to a recorded symbol "1", otherwise the output of the detector will yield the symbol "0". The equalizer block is usually a wideband high-order passive differential low-pass filter used as a pulse-slimming equalization filter for improved performance, it usually combines high-frequency boost with low noise enhancement. The clock recovery and decoder blocks synchronize and decode the user data.

The main features of this scheme are simplicity, low power and low complexity. The main limitation of peak detection read channels is that the data-encoding scheme doesn't allow the use of more aggressive data storage techniques based on the augment of user bit density. This limitation in linear data density strongly compromises the desired storage capacities, whilst maintaining slow data transfer speeds. As data density increases, the flux reversals are packed more tightly and start to interfere with each other, whereas these analog peaks are processed at higher rates, thus significant overlapping occurs, leading to inter-symbolic interference and to data bit errors, timing errors, peak shifts, peak drops. All of these can contribute significantly for the reduction of bit error rates (BER). To reduce interference whilst augmenting bit-density, the magnetic fields must decrease, thus peak detection becomes a week solution, especially at user bit densities pw50/T superior to 1. This has made alternative read channel schemes flourish, and proved them superior to traditional peek detection read channels.

To solve this problem, IBM introduced its first-generation partial-response maximum likelihood (PRML) read channel technology in hard disk-drives in 1990. The PRML approach differs from traditional peak detector read channels, which do not compensate for ISI, by using advanced digital filtering processing to shape the read signal frequency and timing characteristics to a desired partial response, and by using maximum-likelihood digital data detection to determine the most likely sequence of data bits that was written to the disk.

2.2 Partial response maximum likelihood read channels

Partial Response Maximum Likelihood (PRML) coding in magnetic recording was first proposed by Kobayashi *et al.* [1-2] early in 1970 based on Lender's work on correlative level coding [3]. However, only recently has it been monolithically implemented. The main features of PRML are the modeling of the read channel as a linear finite-state machine and the use of maximum likelihood decoding as proposed by Viterby [4], thus allowing increased data rates and user bit density, and hence, augmented disk storage capacity when compared with standard non-return-to-zero (NRZ) and RLL coding peak detection read channels. This performance is achieved with additional complexity and high consumption especially at high data rates. Different classes of partial response read channels [5-10] share the same simplified structure depicted in figure 5.

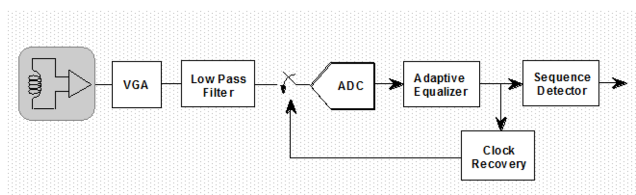


Figure 5. Partial response read channel block diagram

It includes an analog to digital converter (ADC), a digital finite impulse response (FIR) adaptive equalizer, and a Maximum Likelihood Sequence Detector (MLSD), usually a Viterbi algorithm detector is used as an efficient approach to MLSD. Later designs have also included a discrete time FIR forward equalizer after the low-pass filter for precursor ISI removal. The clock recovery circuitry provides the desired sampling rate and phase for the sample and hold block at the ADC input, based on a feedback loop filter and on a Voltage Controlled Oscillator (VCO). The keys to this scheme are fast analog to digital and efficient ISI cancelling on the adaptive equalizer.

The referred partial response (PR) coding is done in the adaptive equalizer, the key block of the read channel. Different approaches to the coding are available although all of them are based on the partial response polynomial shown in (5).

$$P(D) = (1-D)^m.(1+D)^n \tag{5}$$

This delay polynomial derives from the z-transform of the equalizer function where $D = z^{-1}$, and the equalizer complexity is given by number of tapped delays and equal to $m + n$. The differentiating function of the read head on the NRZ pattern is usually given by (1-D) thus most PR schemes use m=1. Coefficients m and n determine the complexity of the equalizer transfer function each corresponding to a variant of PR as shown in table 1.

Table 1. Partial response variants

m	*n*	Coding		
1	0	No coding		NRZI
0	2	Class II	Partial Response	PR2
1	1	Class IV	Partial Response	PR4
1	2	Class IV	Extended Partial Response	EPR4
1	3	Class IV	Extended Partial Response	E^2PR4

2.2.1 Partial response class IV

All partial response read channels assume a fixed well-known model for the read head response to an isolated transition and linear superposition of adjacent transitions. Partial response coding based on m=1 and n=1, denominated Class IV or simply PR4, is a simple and elegant realization of PR, where each voltage pulse results in two samples, thus delaying the decision in time, as given by PR polynomial

$$P(D) = (1-D)\cdot(1+D) = 1-D^2 \,. \tag{6}$$

In the late nineties several PRML-based solutions for the read channel were proposed [11-18] all employing advanced and aggressive analog to digital converters, allowing areal densities to increase by up to 50% when compared to conventional peak detection channels. Greater overall capacities and faster transfer bit rates rapidly pushed these read channels as the new standard for data decoding on modern hard disks. Extended versions of PRML with longer partial response polynomials, such as EPRML and E^2PRML, using much more complex implementations of the maximum likelihood algorithm, also became available.

2.2.2 Extended partial response class IV

An improved solution using m=1 but setting n=2 further extends the response in time, given that each isolated pulse results in a sequence of three voltage samples (1,2,1) as a consequence of the quadratic form of term $(1+D)^2$ on equation (5). This PRML codding technique is designated as extended partial response Class IV, or EPR4 and is given by equation

$$P(D) = (1-D)\cdot(1+D)^2 = 1+D-D^2-D^3 \,. \tag{7}$$

The use of a better algorithm and more complex signal-processing allowed a more than 20% increase in linear density, and hence in areal density, without increasing BER. Further development of PR class IV using m=1 and n=3 as given by

$$P(D) = (1-D)\cdot(1+D)^3 = 1+2D-2D^3-D^4 \tag{8}$$

has been proposed and several viable solutions [19-27] have been presented to implement the read channel. Read channels using this coding scheme, designated as E^2PRML or E^2PR4, have allowed the augment of total disk capacity, and consequently have been widely adopted in the hard disk industry replacing PRML. E^2PR4 systems can also take advantage of density gains and combine RLL(1,7) encoding with non-return-to-zero inverted (NRZI) modulation. Several PR employing d=0 run length constraint have also been presented to reduce the complexity of the detector whilst attaining higher code rates. E^2PRML equalisation can reduce critical requirements such as high frequency, although extended PRML schemes increase circuit complexity and require higher resolution for the ADC. Fast suboptimal simplified Viterbi detectors are usually used since the complexity of MLSD increases exponentially with the number of tapped delays. Unfortunately, high transfer rates imply costly consumption requirements since power consumption in digital blocks is roughly proportional to the signal frequency, and hence to the data transfer rate, this is particularly important in the case of portable systems where power consumption is the key to balance speed and battery operation autonomy. Table 2 summarizes the most relevant characteristics of proposed PRML read channels showing the available results for data rate, power consumption, die area and technology.

Table 2. PRML channel evolution

Year	Technology	Data Rate		Power	Area
1994	0.8µm BiCMOS	8/9	100 Mb/s	0.80 W	–
1994	0.8µm CMOS	8/9	72 Mb/s	1.50 W	–
1994	0.8µm CMOS	8/9	36 MHz	0.69 W	51 mm^2
1995	0.5µm BiCMOS	10/6	16 MB/s	1.20 W	26 mm^2
1996	0.6µm CMOS	5/6	130 Mb/s	1.35 W	28 mm^2
1996	0.7µm BiCMOS	7/6	150 Mb/s	1.55 W	47 mm^2
1996	0.5µm BiCMOS	8/9	200 Mb/s	0.85 W	20 mm^2
1996	1.0µm CMOS		160 MHz	0.46 W	23 mm^2
1999	0.35µm CMOS[12]		300 MHz	0.23 W	0.8 mm^2
2002	0.18µm CMOS[13]		150 Mb/s	0.18 W	1 mm^2
2006	0.35µm CMOS[13]		300 MHz	–	12.8 mm^2

Various magnetic read-channels based on PRML have been able to meet the increase of data acquisition rates. However, this has been accomplished at the expense of complexity and power dissipation. Performance limitations of PRML solutions based on fast ADC acquisition and bulky signal processing leave short margin for data

[12] Consumption and area values for ADC only [26].

[13] Proposed for optical disc formats, CD, DVD and Blu-ray disk (BD) in [27].

rate increases, thus strongly limiting their application in HDD read channels, although still showing to be robust solutions for optical data systems such as DVD/Blu-ray.

Alternative architecture delivering equivalent performance to the most advanced partial response read channel solutions, were presented based on decision feedback equalization (DFE) using digital FIR filter techniques that avoid high frequency acquisition ADC. In August 1996, Philips Semiconductors announced its first standard RAM-DFE read channel device, a fully-adapted self-training DFE scheme compatible with a wide range of read head and media interfaces. Adaptation allows improved bit-error rate achieving signal-to-noise ratio equivalent to PR4 read channel, at increased user data bit density (superior to 2.0).

2.3 Decision feedback equalization read channels

The Decision Feedback Equalization (DFE) structure was first presented in 1967, by M. Austin as an equalizing technique for dispersive channels, as described in [28]. Adaption capability was further proposed and added to the system in 1971 by D. George *et al.* in [29], but it was only in 1996 that this scheme was firstly integrated in a commercial circuit as a practical alternative to peak detection techniques. This is also the main structure from which derived some of the schemes described onward (such as FDTS/DF, RAM-DFE and MDFE). It basically consists of two equalizing filters and a decision element (slicer) as depicted in figure 6.

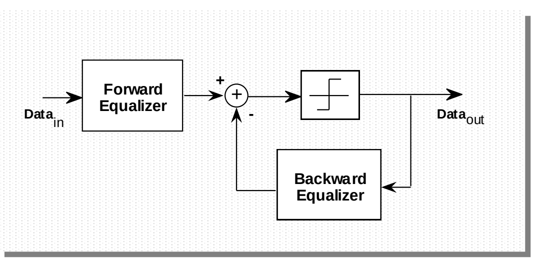


Figure 6. Decision feedback equalization block diagram

The forward equalizer is typically a linear FIR filter used for precursor ISI cancellation and the backward equalizer is a non-linear postcursor ISI remover. The non-linearity in the feedback caused by the decision element ideally enhances noise robustness, although once an error occurs it will propagate to subsequent symbols. One interesting feature of this equalization scheme is the possibility to tune both filter sections. This is usually accomplished using LMS modified algorithms. Consequently tapped delay transversal FIR filters are the natural choice for these blocks due to their ease of implementation and tuning or programming abilities.

2.3.3 RAM decision feedback equalization channel

RAM-based equalization is also used for ISI removal on storage channels, although it was first presented as a non-linear echo canceller for data modems [30]. This technique is particularly effective on channels for which the linear superposition is an inaccurate model. The non-linear effects on postcursor ISI can be canceled by detecting the sequence of the previous symbols and subtracting the corresponding RAM-stored value (for that particular sequence) from the signal at the input of the slicer. The detected sequence is temporarily stored in a shift-register whose outputs decode the RAM element that holds the expected error values, as depicted on figure 7. The stored values can/must be tuned recursively to improve equalizing performance although this can prove to have convergence problems and comparatively higher complexity then adaptive linear equalizers. The forward filter is a linear equalizer, usually a FIR filter as those used in conventional DFE read channels.

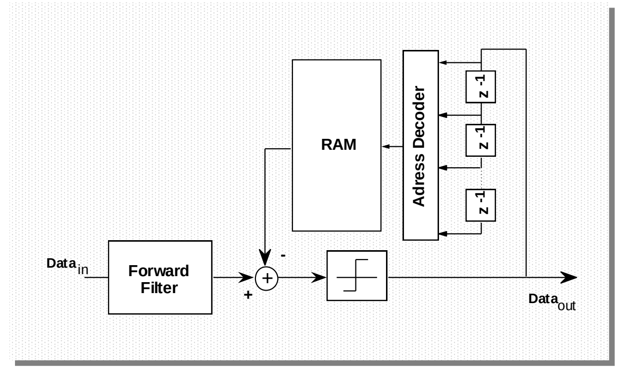


Figure 7. Block diagram of a RAM-based decision feedback read channel

In linear echo cancellation, the assumption for canceling causal ISI using linear equalizers is that a linear superposition of the previously detected symbols will model the total echo on the current symbol. This principle suggests the use of transversal FIR filters for this purpose as was described previously. Alternatively non-linear cancellation as proposed by Agazzi *et al*. [31] assumes echo signals to be a non-linear function of the current and past symbols, requiring the channel to be time invariant, and also suggesting the use of memory elements. The first DFE equalizer using RAM-Based equalization was published in 1989 by Fisher *et al* [32-33] but its hardware complexity as kept it away from the disk-drive market, moreover with the high linearity behavior of magneto resistive read heads at high densities. Nevertheless, a publication by Sands *et al.* [34] reporting a 200 MHz RAM-DFE channel using a linear adaptive tapped delay forward filter and a non-linear adaptive backward equalizer comprising a RAM element and a linear adaptive equalizer led to the launch of a standard RAM-DFE read channel by Philips in 1996. In a later publication Brown and Hurst [35] propose a complete RAM-DFE chip with 11.2 mm^2 operating at 80 Mb/s and dissipating 630mW using a first order continuous-time forward equalizer and a 4-tap FIR backward equalizer.

2.3.4 Fixed-delay tree search with decision feedback channel

The Fixed-Delay Tree Search with Decision Feedback (FDTS/DF) equalizer was first presented in 1988, by J. Moon and L. Carley [36-38] as a quasi-optimum implementation of a Maximum-Likelihood Sequence Detector (MLSD) for Run-Length-Limited (RLL) with a decision element similar to partial response. The equalizer basically consists on a forward and a backward filter, along with a FTDS decision block. Usually a FIR filter is used as a forward equalizer to cancel the precursor ISI, although adaptive analog implementations can lower the power consumption needs. Causal ISI is eliminated using a feedback filter as in DFE, but the weights of the feedback taps are smaller than its DFE counterparts thus reducing error propagation. The complete block diagram is depicted in figure 8 including the LMS algorithm block used to make the forward equalizer adaptive.

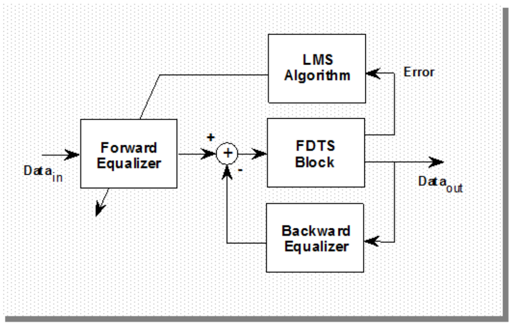


Figure 8. Block diagram of a
Fixed Delay Tree Search with decision feedback read channel.

The decision delay goal is to look ahead some symbols before making the decision, according to an exhaustive tree-search, as the one shown in figure 9. Similarly to a Viterbi detector, the most likely path (or sequence) is determined by minimizing the Euclidean distance between predictable and detected sequences.

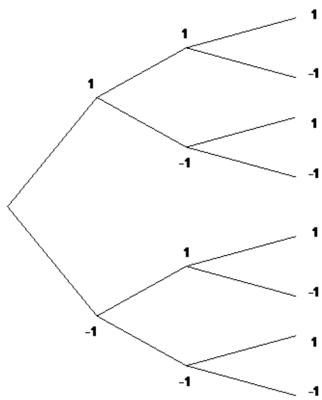


Figure 9. Binary tree search structure

The FTDS algorithm achieves near-optimum performance in the case of RLL constrained input sequences since the critical error events are short and invalid paths are of easy detection, making it of reasonable hardware complexity and cost, with a performance close to that of MLSD. The *d* constrain in RLL (1,7) code significantly reduces the number of possible paths and the complexity of the decision tree. Moreover, low-end drives have prompted considerable efforts for the development of low power continuous-time adaptive equalizer solutions alternative to the digital FIR approach usually used with DFE read channels. Several studies [39-42] led to the proposal of Multilevel Decision Feedback Equalization (MDFE), and in February 1995, Kenney suggested the development of an allpass continuous-time filter solution for the realization of the forward equalizer with equivalent performance to that of a long tapped-delay FIR filter as the key block of MDFE.

2.3.5 Multilevel decision feedback equalization channel

Multilevel Decision Feedback Equalization was first presented in 1993, by Kenney *et al* [43-45] as a quasi-optimum implementation of a Maximum-Likelihood Sequence Detector (MLSD) for Run-Length-Limited (RLL) systems. The block diagram of MDFE depicted in figure 10 is similar to that of FTDS/DF, also comprising a forward and a backward filter, but using a simple slicer instead of a FTDS decision block, just like the other DFE-based systems. However, this results from the simplification of the FTDS decision block, providing the channel uses RLL (1,7) encoded data.

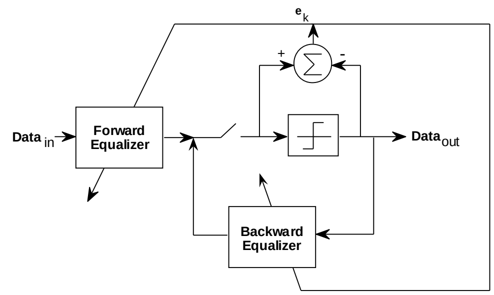


Figure 10. Block diagram of a
Multilevel Decision Feedback Equalization

Usually a FIR filter is used as a forward equalizer to cancel the non-causal precursor ISI, but [46] suggests that an adaptive analog implementation can show equivalent performance to that of a long (24 taps) FIR filter, whilst decreasing power consumption needs. Causal ISI is eliminated using an equalizing filter in the feedback loop, just as in DFE but also with reduced weights of the feedback taps. Table 3 comprises several equalizers proposed for implementation the forward equalizer in PRML and DFE read channels.

Table 3. Equalizer evolution[14]

Year	Technology		Freq.	Power	Area
1993	1.0µm CMOS	SC-FIR	7.1 MHz	988 mW	146 mm^2
1993	2.0µm CMOS	SC-FIR	40 MHz	500 mW	31 mm^2
1994	0.8µm CMOS	A-FIR	72 MHz	500 mW	–
1994	1.2µm CMOS	SC-FIR	100 MHz	900 mW	44 mm^2
1995	0.5µm BiCMOS	D-FIR	200 MHz	690 mW	4 mm^2
1995	0.8µm CMOS	A-FIR	240 MHz	426 mW	2.9 mm^2
1996	0.6µm CMOS	SC-FIR	200 MHz	507 mW	13 mm^2
1997	0.8µm BiCMOS	A-FIR	160 Mb/s	200 mW	1.4 mm^2
1997	0.5µm CMOS	gm-C	100 MHz	3 mW	0.06 mm^2
1997	0.6µm CMOS	gm-C	150 Mb/s	90 mW	0.8 mm^2
1998	0.25µm CMOS	A-FIR	360 Mb/s	21 mW	0.06 mm^2
1999	1.0µm CMOS	A-FIR	80 Mb/s	280 mW	6.7 mm^2
2002	0.5µm CMOS	A-FIR	100 Mb/s	130 mW	1.3 mm^2
2005	0.18µm CMOS	gm-C	70 MHz	21.8 mW	–
2007	0.18µm CMOS	gm-C	400 MHz	190 mW	–
2008	0.18µm CMOS	gm-C	400 MHz	80 mW	–

14 SC-FIR denotes discrete time FIR tapped delay filter using switched-capacitor delay cells.

A-FIR denotes discrete time FIR tapped delay filter using gm-C or OTA-C to implement the delay cells.

D-FIR denotes discrete time digital FIR filter.

gm-C denotes continuous time gm-C filter.

Cited equalizers [57-73] use different filtering techniques.

It is of considerable interest that both filters operate in current-mode so that the outputs of these filters are added in the current summing node that precedes the sampling switch. The adaptation process depends on the generation of the error signal estimated by the difference between the prediction value at the input of the slicer and the data decision at its output.

For the implementation of a 3rd order allpass continuous-time adaptive equalizer [47-49], designed to work at very high frequency at low power consumption - less than one tenth of traditional FIR power needs - and low supply voltage, the design option was to use adaptive state-space recursive filters based on current-mode Gm-C structures employing low-mismatch high bandwidth pseudo-differential balanced transconductors and polarized MOSFET arrays as integrating capacitors.

3. AVAILABLE TECHNIQUES FOR THE EQUALIZER

A previous theoretical work [46] based on MATLAB simulation for a 100 MHz sampling frequency can be used to derived ideal pole locations for the forward equalizer. For a third order system, the pole positions maximizing performance can be show to be:

Real Pole	f =	8 MHz	
Complex Poles	f_0 =	26 MHz	Q = 0.6

and hence, the system transfer function can be expressed by

$$H(s)=\frac{-S^3+3.26\cdot10^8S^2-4.1308\cdot10^{16}S+1.3754\cdot10^{24}}{S^3+3.26\cdot10^8S^2+4.1308\cdot10^{16}S+1.3754\cdot10^{24}} \quad (9)$$

3.2 Adaptive Gm-C Architectures

For the above specifications, two Gm-C current-mode structures were designed and compared based on transistor level simulations. Both architectures adapt using LMS modified algorithms [50-56], and allow the parasitic input capacitance in the Gms to be taken into account for very high frequency operation. The automatic tuning of the poles frequency also compensates process tolerances that influence the effective value of the active devices and capacitors. The equalizers linearity is mainly determined by the linearity of the transconductors and integrating capacitors. The DC voltage inherent to the simulated structures biases these transistors well beyond their threshold voltage for enhanced linearity behavior.

2.2.1 Canonical Structure

Firstly, we considered the canonical structure illustrated in figure 11. It is composed of four equal value pseudo-differential transconductors embedded in a grounded capacitive network.

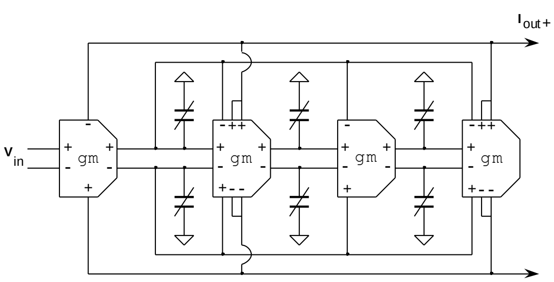


Figure 11. Canonical structure

The corresponding 3rd order current mode state-space recursive system can be expressed as

$$\begin{cases}[\dot{i}]=[A]\cdot[i]+[B]\cdot i_{in}\\ i_{out}=[C]^T\cdot[i]+D\cdot i_{in}\end{cases} \quad (10)$$

where the system matrices are given by

$$[A]=\begin{bmatrix}-gm_0/C_0 & -gm_0/C_0 & -gm_0/C_0\\ gm_1/C_1 & 0 & 0\\ 0 & gm_2/C_2 & 0\end{bmatrix} \quad (11)$$

$$[B]=\begin{bmatrix}gm_0/C_0\\0\\0\end{bmatrix} \quad (12)$$

$$[C]=\begin{bmatrix}2\\0\\2\end{bmatrix} \quad (13)$$

$$D=-1 \quad (14)$$

Notice that matrix [A] assumes the typical *row-shape* characteristic of canonical structures. The system transfer function is thus given by

$$H(s)=\frac{-S^3C_0C_1C_2+S^2C_1C_2gm-SC_2gm^2+gm^3}{S^3C_0C_1C_2+S^2C_1C_2gm+SC_2gm^2+gm^3} \quad (15)$$

Considering equal-valued transconductors with a nominal transconductance value of 60 μS and after subtracting the effect of the parasitic input capacitance of the Gms we obtain the following nominal values for the integrating capacitors

C_o = 0.083pF, C_1 = 0.47pF, C_2 = 1.8pF.

2.2.2 Orthonormal Structure

In alternative to the canonical structure described before we also considered the orthonormal structure represented in figure 12. Although the design of the orthonormal structure is usually a more complex approach, it can take a rather simplified format for the allpass filter. Moreover, it uses only one of the state variables to build the allpass current output wave and thus making it more immune to noise and offset problems than the previous canonical structure.

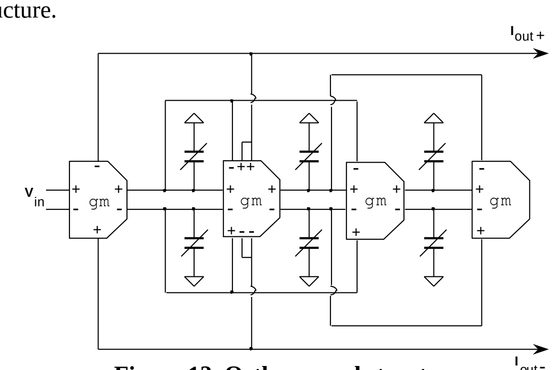


Figure 12. Orthonormal structure

The corresponding 3rd order state-space system is also expressed by matrix equation (10) but the system matrices are now given by

$$[A]=\begin{bmatrix} -gm_0/C_0 & -gm_0/C_0 & 0 \\ gm_1/C_1 & 0 & -gm_1/C_1 \\ 0 & gm_2/C_2 & 0 \end{bmatrix} \quad (16)$$

$$[B]=\begin{bmatrix} gm_0/C_0 \\ 0 \\ 0 \end{bmatrix} \quad (17)$$

$$[C]=\begin{bmatrix} 2 \\ 0 \\ 0 \end{bmatrix} \quad (18)$$

$$D=-1 \quad (19)$$

A simple scaling of the system state-variables would transform it in the orthonormal ladder structure proposed in [53]. Hence, since the filter satisfies Lyapunov's equation

$$AK+KA^T+2\pi bb^T=0 \quad (20)$$

all the system state-variables are orthogonal and the dynamic range is optimized. The system transfer function for the structure in Fig. 3 is given by

$$H(s)=\frac{-S^3C_0C_1C_2+S^2C_1C_2gm-S(C_0+C_2)gm^2+gm^3}{S^3C_0C_1C_2+S^2C_1C_2gm+S(C_0+C_2)gm^2+gm^3} \quad (21)$$

Considering again equal-valued transconductors with the same nominal value of 60 μS and after subtracting the effect of the input capacitance of the Gms we obtain the following nominal values for the integrating capacitors

C_0 = 0.102pF, C_1 = 0.49pF, C_2 = 1.77pF.

3.3 Adaptive Capacitor Array

The adaptation of the Gm-C filters previously described is achieved by means of integrating capacitor structures C_i consisting of a constant *course* MOSFET capacitor C_i' in parallel with an N-bit digitally controlled *fine* tuning capacitor array C_i, as shown in figure 13.

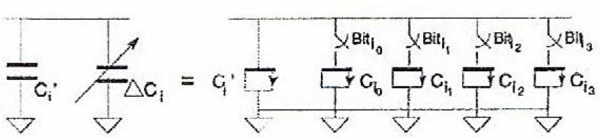


Figure 13. Integrating capacitors are formed by a fixed capacitor in parallel with a digitally controlled capacitor-array.

the total integrating capacitance is given by

$$C_i = C_i' + \Delta C_i \quad (22)$$

where

$$\Delta C_i = \sum_{k=0}^{N} C_{ik} \cdot Bit_{ik} \quad (23)$$

and

$$C_{ik} = 2^k \cdot C_{iN} \quad (24)$$

thus can be expressed as

$$\Delta C_i = C_{iN} \cdot \sum_{k=0}^{N} 2^k \cdot Bit_{ik} \quad (25)$$

The minimum value C_i' and the maximum value $C_i' + max(\Delta C_i)$ of each integrating capacitor C_i are dimensioned to allow the desirable placement of the poles, even under worst case process tolerances that influence the actual value of Gms and of the integrating capacitors. The number of adaptation bits must provide sufficient adaptation precision of the arrays without unduly increasing the circuit complexity. For both structures described before we considered N = 4-bit capacitor arrays made of biased 12.5 fF unit size transistor cells that can be switched on and off by the adaptive control logic. The adaptation process is assumed to be done during the clock recovery preamble and be stable at the decision instants. Alternatively the capacitor array can be loaded in parallel and subsequently adapted to optimum values.

3.4 Transconductors

The transconductors employed in the above filters are based on balanced pseudo-differential lossy-C structures, as shown in figure 14. Unlike in the circuit used in [57-58], biasing is provided by the feedback loops established in the filter, yielding improved stability and noise immunity. Moreover, the transistors dimensions determining the biasing voltages were calculated to minimize the allowed mismatch while maintaining maximum frequency performance. Computer simulations showed that such transconductors are capable of maintaining the correct operation of the filter for supply voltages as low as 1.8 V.

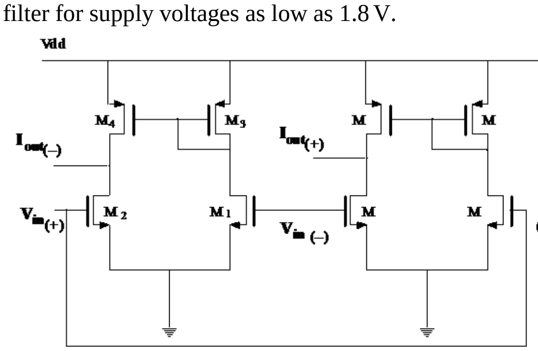
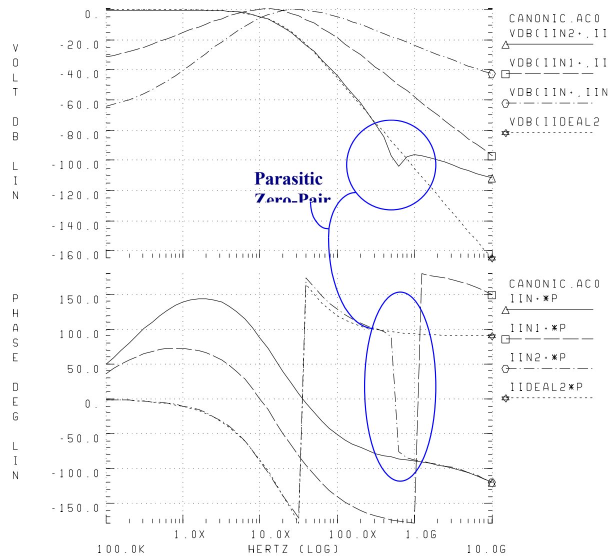


Figure 14. Balanced pseudo-differential transconductor.

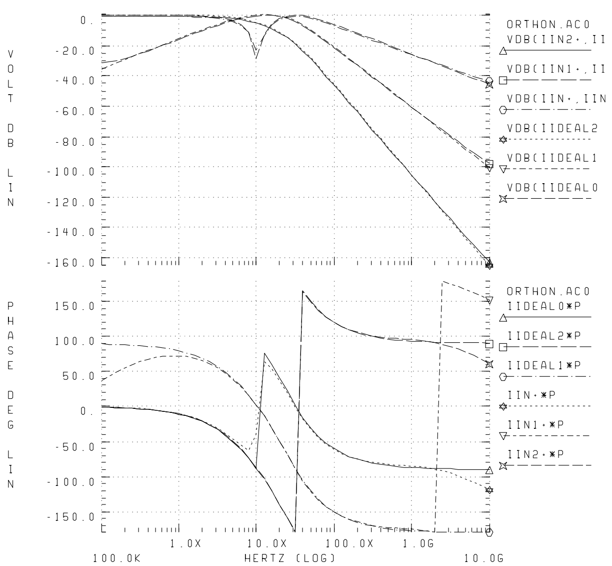
3.5 Results and Discussion

3.5.6 Frequency Response

Transistor level simulations of both structures with nominal integrating capacitance values produce the amplitude and phase versus frequency response characteristics shown in figure 15.(a) and figure 15.(b), respectively for the canonical and orthonormal structures. Whereas with the response of the canonical structure there is a parasitic zero-pair mismatch in state variable I_{in2} around 450MHz in the orthonormal structure all state variables I_{Ini} nearly match the ideal I_{Ideali} amplitude and phase characteristics well over 1GHz.



(a)



(b)

Figure 15. Frequency response of the (a) canonical and (b) orthonormal filter structures, for nominal integrating capacitance values

This shows that under identical design conditions the orthonormal structure has a better high frequency performance behavior. Besides, the orthonormal structure has improved adaptability capabilities since it allows independent pole tuning.

3.5.7 Transient Response

The transient response of both structures was analyzed using an input corresponding to measured data from the magnetic read head. Waveshape V_{in} represents consecutive transitions, one up and one down, usually mentioned as dibit response. The resulting equalized transient response of the orthonormal and canonical outputs are superimposed and are both represented by I_{real} in figure 16, showing that both structures practically match the predicted response from the ideal implementation I_{Ideal}.

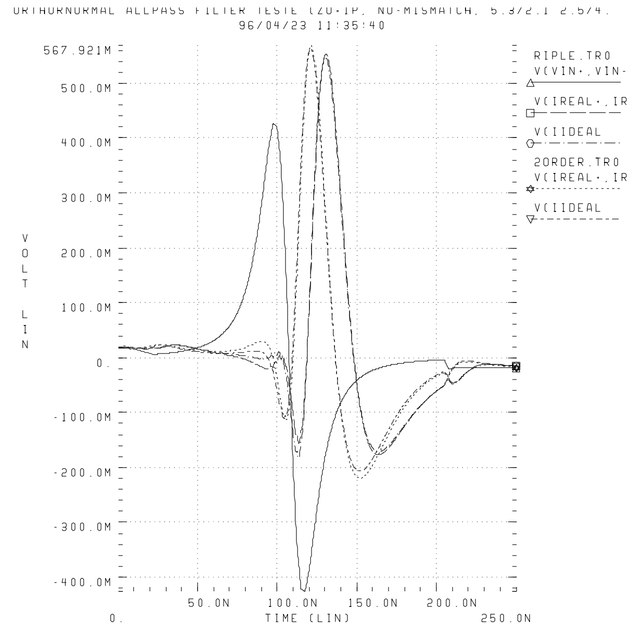


Figure 16. Dibit-response of the allpass filter

4. CONCLUSIONS

This paper presented the most relevant read-channel equalization techniques used in hard disk drive storage. Basic principles and key concepts are introduced along with the building blocks of disk drive electronics. The main read channel architectures alternative to peak-detection: PRML-based and DFE-based are described and compared. Two fully analog continuous-time integrated adaptive filters are proposed for the implementation of an allpass forward equalizer for MDFE read channels. An orthonormal current mode state-space recursive filter is proposed and shown superior at transistor level to a companion-form equivalent canonical structure. Current mode continuous-time gm-C filters using auto-biased transconductance cells operating at very high frequency combined with biased MOSFET capacitor arrays in standard digital CMOS technology are proposed, Operating with supply voltages as low as 1.8 V, whilst reducing consumption by a factor of 10 to 100 compared to conventional FIR digital equalizers exhibiting equivalent performance.

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