A Continuous-Time Area Detector Servo Demodulator for Hard Disk Drives

Nuno de Figueiredo Garrido and José E. Franca

Department of Electrical and Computer Engineering, Integrated Circuits and Systems Group
Av[a] Rovisco Pais, 1, 1096 Lisboa Codex, Portugal
+351-1-8418095, +351-1-8417675
garrido@ecsm4.ist.utl.pt, franca@ecsm4.ist.utl.pt

ABSTRACT*

This paper presents a continuous-time servo demodulator for magnetic disk drives implemented as a programmable current-mode operated Gm-C filter. This first order filter consists of pseudo-differential balanced transconductors and of a MOSFET bank array to implement a variable integrating capacitor. Simulation results are presented.

1. INTRODUCTION

Servo information is essential to control the positioning of the actuator exactly on track and precisely regulate the rotation speed of the spindle. The classic servo controller functionality requires both analog and digital circuitry and can be implemented in a single slave IC device or integrated with other disk drive functions, such as digital signal processor (DSP), ADC, DAC, frequency synthesizer, precision voltage reference [1][2][3][4][5][6]. Whereas historically mass storage multi-disk hard drives often provided a separate platter surface just for servo using dedicated head and pulse detector channel, modern single disk drives with embedded servo provide all necessary information in servo designated sectors, as shown in Fig. 1.

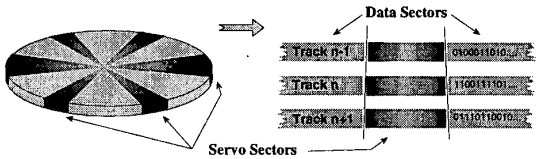

Fig. 1. Servo sectors in the hard disk.

These servo sectors are evenly distributed along the disks surface, interleaved with data sectors, in such a way that practically constant monitoring of the read head positioning is assured, without unduly decreasing usable space and data transfer speed. The format of the information contained in these sectors depends on the manufacturer, but typically consists of three distinct fields with special characteristics: preamble, Gray code, and servo bursts — A , B , C , D , according to Fig. 2.

Fig. 2. Servo sector information format.

The preamble field consists of alternate positive and negative pulses used during automatic gain control (AGC) to calibrate the variable gain amplifier (VGA), and to lock the servo demodulation circuitry to the data stream so that the Gray code field may be read correctly. This field together with a servo mark (not shown in the diagram) asserts that the magnetic head is in the servo sector. The Gray code field contains identification data such as servo field ID, track number, general purpose ID, head ID. This data is usually encoded as run-length limited (RLL) code in various formats. The data is acquired and decoded by the servo demodulator and subsequently transmitted to the DSP. While the track number is used to control the coarse position of the read head, the servo bursts confer its fine positioning on track. The servo bursts are specially written zones on the disk that are intentionally offset by fixed amounts with the center of the track as depicted in Fig. 3. A linear signal is produced by the processing of these bursts as the head moves off-track in either direction from the track center.

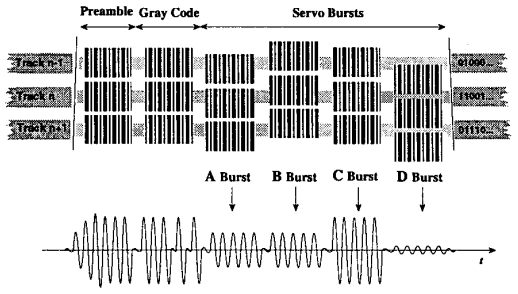

Fig. 3. Servo bursts field format.

Hence, the amplitude of the read signal is proportional to this misalignment, showing maximum peak-to-peak voltages when the head is exactly centered on track and minimum values when it is between two adjacent tracks.

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Typically four sub-fields are used: two symmetrically offset (A) and (B), one exactly centered on track (C), and one in-between tracks (D), although these fields vary depending on the disk drive manufacturer [7]. The controller estimates the position of the read head relatively to the center of the track by comparing the amplitudes of these bursts, e.g. by keeping the amplitudes of A and B equal. This feedback control is dependent on accurate amplitude assessment and therefore an analog-to-digital converter is required. The servo demodulation channel usually works at less than half of the read channel data frequency and only during the servo field sector, hence, simplified architectures have been presented [8][9] that take advantage of time interleaving to share most of the blocks necessary for each of these channels, thus building read/write channels with integrated servo demodulation. The tendency to reach for minimum cost systems, especially important in low end products, makes this solution attractive and further pushes for completely integrated functionality in a single mixed signal CHIP, combining all referred auxiliary blocks, a digital processor and combined servo and data channels.

2. AREA DETECT SERVO BURST DEMODULATOR

The peak detection demodulator architecture has been held up from the classic peak detection read channels and basically contains an input VGA, a continuous-time low-pass filter (LPF), an optional rectifier block and a peak-detector circuit, followed by an analog to digital converter (ADC). The peak-detection block is usually a clamper circuit whose analog output level is quantified at the sampling instants by the ADC and dispatched to the processor. Alternatively, a synchronization circuit can be used to sample the pulses at their peak voltages. Area demodulation can be obtained by replacing the peak-detection block by a continuous-time integrator, as shown in Fig. 4.

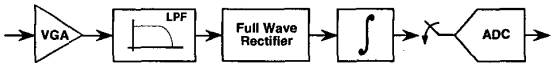

Fig. 4. Area detect servo burst demodulator architecture.

Averaging the contribution of several pulses eliminates the dependence of the sampled voltage on the shape of the last pulse and can easily be processed asynchronously. Moreover, the voltage sample is inherently held in the capacitor bank and subsequently acquired at a programmable instant near the end of each burst, as depicted in Fig. 5.

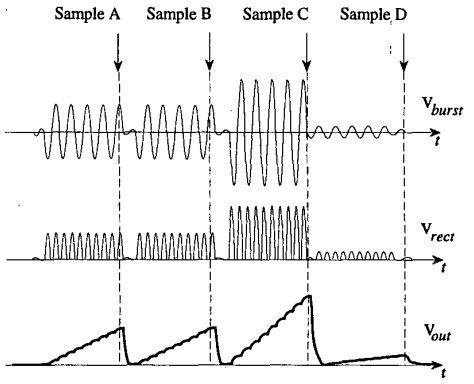

Fig. 5. Area detect servo burst demodulation waveforms.

Continuous-Time Integrator

The programmable Gm-C filter proposed for the implementation of the area integrator block is shown in Fig. 6. It is a fully-balanced current-mode structure consisting of two transconductors and of a MOSFET capacitor bank array C_i. Transconductor gm_0 converts the input voltage to current, while capacitor array C_i and transconductor gm_1 realize the continuous-time integrator.

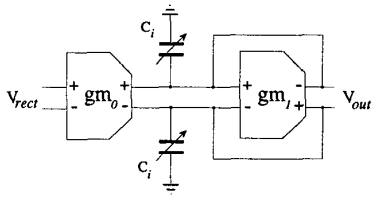

Fig. 6. Area integrator implementation.

At design level, gm_0/gm_1 ratio establishes the nominal gain of the integrator and its power consumption. Likewise, programming C_i allows additional flexibility and accurate control of the integrated signal for a large range of operating frequencies and for a variable number of utilized burst cycles. The integrator schematics depicted in Fig. 7 embody an high frequency auto-biased transconductor that uses current feedback to set the pole of the filter while stabilizing the common mode voltage, as described in [10]. The estimated area of the rectified pulse stream is assessed differentially at the current summing nodes I_{rect-} and I_{rect+}. Following the ADC acquisition, an auxiliary switch quickly resets the capacitor bank so that the next burst can be integrated.

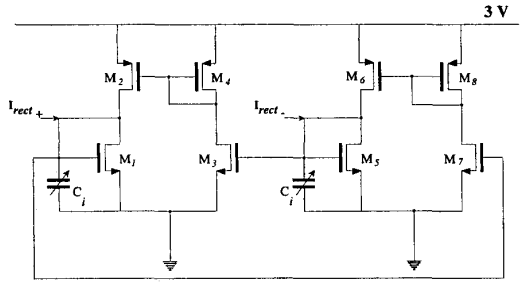

Fig. 7. Balanced pseudo-differential integrator.

Programmability and Gain Adjustment

The referred gain adjustment is performed by the integrating capacitor array C_i, as is similarly described in [11][12][13]. The DSP initially loads and subsequently adapts the capacitor array according to the feedback information given by the amplitudes of A, B, C, D. This tuning procedure also neutralizes deviations due to fabrication tolerances and occurs at lower speed to assure stability. The integrating capacitor C_i combines a binary weighted MOSFET array of 250 fF unit size cells, connected in parallel and digitally controlled by MOS switches, as shown in Fig. 8.

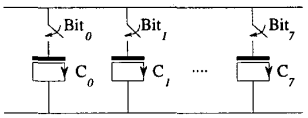

Fig. 8. The integrating capacitor consists of a digitally controlled capacitor-array.

An 8-bit structure provides sufficient precision and versatility at fairly low complexity overhead. The capacitance value is imposed by the hexadecimal vector in the digital bus and is given by

$$C_i = \sum_{k=0}^{7} C_k \cdot Bit_k \text{ , with } C_k = 2^k \cdot C_7 \text{ .} \qquad (1)$$

Consequently, C_i can take any value in the range

C_{min}= 0.250pF = $2^0 \cdot 250$fF (code 00H)

C_{max}= 63.75pF = $(2^8\text{-}1) \cdot 150$fF (code FFH)

The operating frequency scope is hence larger than two decades and upper limited by the parasitic input capacitance of the transconductance cell. The self imposed common mode voltage of the transconductances biases these transistors beyond their threshold voltage for enhanced linearity behavior.

3. Results and Discussion

Frequency Response

Transistor level simulation of the area integrator circuit for integrating capacitance values of 10 pF to 40 pF, produce the amplitude and phase versus frequency response characteristics shown in Fig. 9. The plot of the integrated voltage between nodes I_{rect-} and I_{rect+} indicate that the filter behaves as an integrator in the band of interest, showing a second pole near the *ft* of the transistors as described in [10].

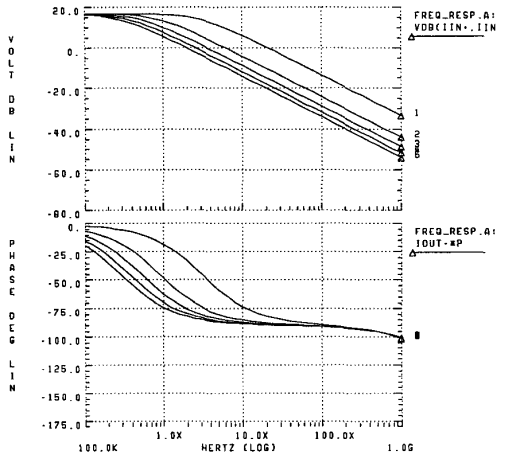

Fig. 9. Frequency response of the area integrator for nominal integrating capacitance values.

Transient Response

The plot in Fig. 10 shows the transient response of the integrator to a five cycle long burst for the same capacitance values. A 10 MHz rectified pulse sequence consisting of measured data obtained from an actual read head has been used to simulate the input servo burst. The optimum compromise between the minimum number of used pulses and the output precision depends on the channel frequency and can ultimately be tuned by the DSP through feedback control of the capacitor array.

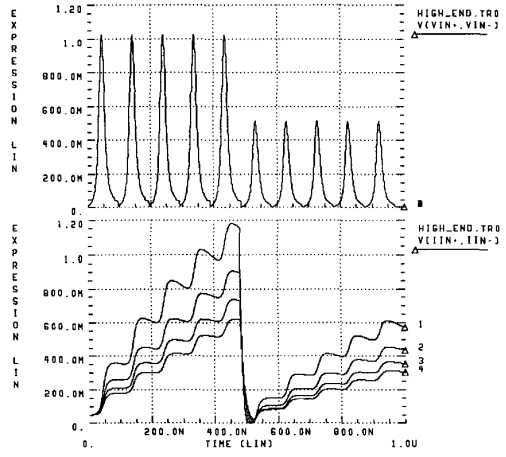

Fig. 10. Transient response of the area integrator to a sequence of Lorentzian pulses for integrating capacitance values of 10pF, 20pF, 30pF, 40pF.

Table I. Main characteristics of the area integrator filter.

Technology	0.5μm Digital MOS
Pole Frequency	1 to 100 MHz
CMRR	80 dB
PSRR, GSRR	60 dB
THD	– 50 dB
Power supply	3.0 V
Power dissipation	3.0 mW
# Tuning Bits	8
Active area	0.2x0.3 mm^2

Table I. summarizes the overall performance attained by simulation of the area detector circuit using a supply voltage of 3.0 V. However, simulations show that the circuit can maintain functionality for lower supply voltages, such as 1.8 V.

4. CONCLUSIONS

The overall development goal in disk drive technology is clearly to reduce device size and power consumption, and to increase data rates and storage capacity. An approximately exponential evolution has characterized the performance of this market with respect to these requirements. The predictable future for low-performance drives is that a single low power mixed-signal CMOS integrated circuit will include all of the necessary electronic blocks. A continuous-time solution for servo burst demodulation using area detection has been presented. In the servo circuits averaging the contribution of several pulses reduces random noise sensibility and eliminates the dependence of the sampled voltage on the shape of the last pulse. This scheme can easily be processed asynchronously requiring only a small number of cycles for each servo burst. The circuit features a flexible low-power and small size die, and can easily be embedded in a read channel with integrated servo controller.

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